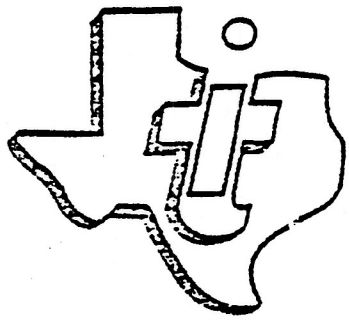


TMS 9918A/9928A/9929A

VIDEO DISPLAY PROCESSORS

PRELIMINARY

SPECIFICATION

OCT, 1981

ADVANCE INFORMATION

This information describes the design specifications for a product under development. Texas Instruments reserves the right to change these specifications in any manner, without notice.

The TMS 9918A/9928A/9929A video display processors (VDP) are N-channel MOS LSI devices used in video systems where data display on a raster-scanned home color television set or color monitor is desired. The TMS 9918A/9928A/9929A generate all necessary video, control, and synchronization signals and also control the storage, retrieval, and refresh of display data in the dynamic screen refresh memory. The interfaces to the microprocessor, refresh memory, and the TV require a minimum of additional electronics for the TMS 9918A.

The TMS 9928A/9929A video display processors are identical to the TMS 9918A VDP with the exception that the NTSC color encoding circuitry has been removed and replaced with luminance and color difference signals. Except for three pins, the composite video output, the external video input and the CPU clock output, the TMS 9918A is pin for pin compatible with the TMS 9928A/9929A. These pins are replaced with the Y (B/W luminance and comp. sync.) output and two color difference pins, R-Y output and B-Y output. The color difference outputs allow the user to generate RGB drive for direct color gun control. However, to connect these three outputs to a monitor requires additional encoder circuitry.

The TMS 9918A/9928A have 525 line format for U.S. televisions while the TMS 9929A has a 625 line format VDP for use with two types of European encoding; PAL (German system) and SECAM (French system).

The VDP has four video display modes: Graphics I, Graphics II, Multicolor and Text mode. The Text mode provides twenty-four 40-character rows in two colors and is intended to maximize the capacity of the TV screen to display alphanumeric characters. The Multicolor mode provides an unrestricted 64 X 48 color dot display utilizing 15 colors plus transparent. The Graphics I provides a 256 X 192 pixel display for generating pattern graphics in 15 colors plus transparent. The Graphics II mode is an enhancement of Graphics I mode, providing the capability to generate more complex color and pattern displays.

The video display consists of 35 planes, external VDP, backdrop, pattern plane, and 32 Sprite Planes. The planes are vertically stacked with the external VDP being the bottom or innermost plane. The backdrop plane is the next plane followed by the pattern plane that contains Graphics I and Graphics II patterns with the 32 Sprite Planes as the top planes. (A sprite is an object-oriented animation pattern that can be moved smoothly across the screen.)

The TMS 9918A/9928A/9929A VDPS utilize either a 4K, 8K, or 16K-type low-cost dynamic memory (TMS 4027, TMS 4108, TMS 4116) for storage of the display parameters.

The TMS 9918A, TMS 9928A and TMS 9929A interface identically to the host microprocessor making them software compatible. Thus, all references to VDP in this document apply to all three devices, except where noted.

2.3.2 TMS 9928A/9929A MONITOR INTERFACE

The Y, R-Y and B-Y output signals require external encoder circuitry to drive a video color monitor; an R-G-B matrix is required to drive R-G-B color monitors. The Y output signal contains all necessary horizontal and vertical synchronization signals as well as luminance while the R-Y and B-Y signals contain the chrominance information. The internal output buffer devices on these pins are source-follower MOS transistors that require an external pull-down resistor to V_{SS} as shown in Figure 2-5. Typically a 560 ohm resistor is recommended.

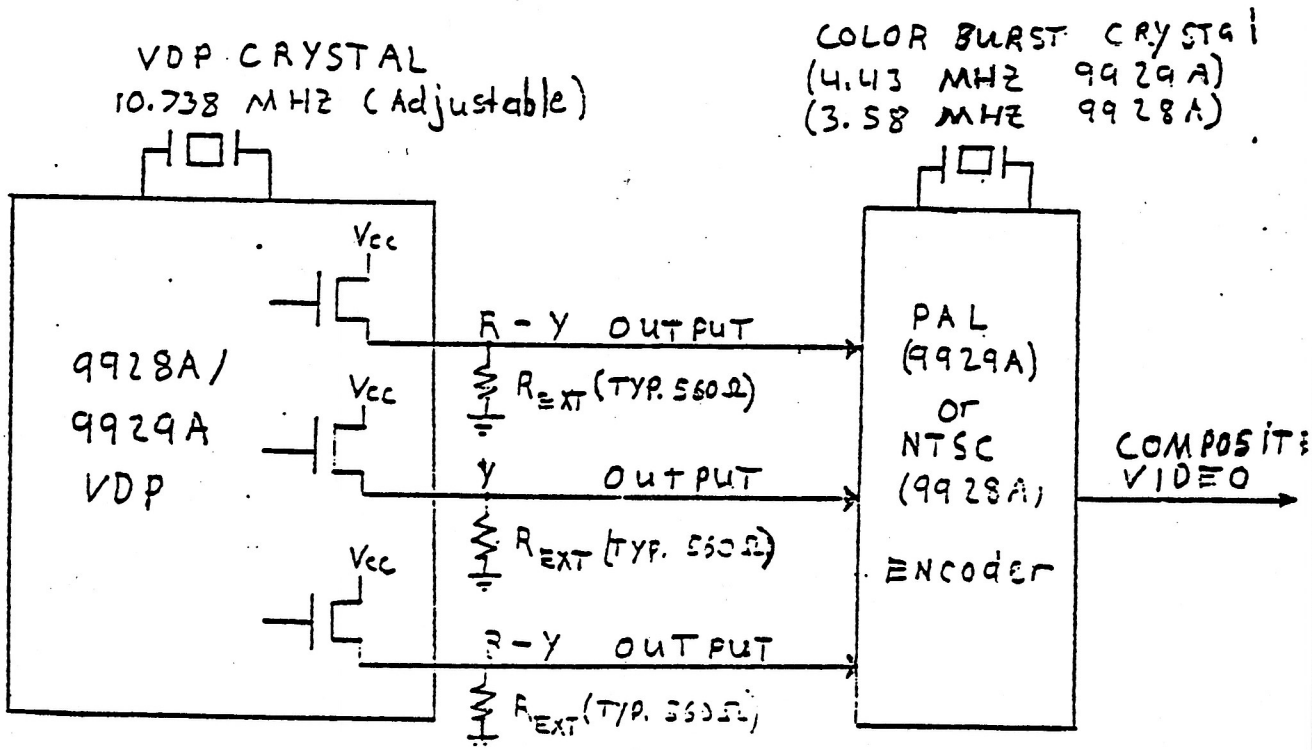


FIGURE 2-5 - TMS 9928A/9929A INTERFACE
* note the LM1889 is typically used in the encoder ciruitry

TABLE 3. COLOR ASSIGNMENTS

(HEX) color	LUMINANCE (DC value)	CHROMINANCE (AC VALUE)	Y	COLOR DIFFERENCE R-Y	B-Y
TRANSPARENT	0.00	—	—	—	—
BLACK	0.00	—	0.00	.47	.47
MEDIUM GREEN	.60	.60	.53	.07	.20
light Green	.80	.53	.67	.17	.27
Dark Blue	.47	.73	.40	.4	1.00
light Blue	.67	.60	.53	.43	.93
Dark Red	.53	.53	.47	.83	.30
Cyan	.80	.73	.73	0.00	.70
Medium Red	.67	.73	.53	.93	.27
Light Red	.80	.73	.67	.93	.27
Dark yellow	.87	.53	.73	.57	.07
light yellow	1.00	.40	.80	.57	.17
Dark green	.47	.60	.47	.13	.23
magenta	.60	.47	.53	.73	.67
Gray		—	.80	.47	.47
white	1.00	—	1.00	.47	.47
Black level	0.00	—	0.00	.47	.47
color burst	0.00	.40	0.00	.73(240)/.47(284)/.20(294)/-1	
Sync level	-0.40	—	.46	.47	.47

TMS 9918A / 9928A

The ~~VDP~~ operates at 262 lines per frame and approximately 60 frames per second in a non-interlaced mode o operation. The TMS 9929A operates at 313 lines per frame and approxim 50 frames per second.

TABLE 2 – SCREEN DISPLAY PARAMETERS

PARAMSTER	PIXEL CLOCK CYCLES	
HORIZONTAL	PATTERN OR MULTICOLOR	TEXT
HORIZONTAL ACTIVE DISPLAY	256	240
RIGHT BORDER	15	25
RIGHT BLANKING	8	8
HORIZONTAL SYNC	26	26
LEFT BLANKING	2	2
COLOR BURST	14	14
LEFT BLANKING	8	8
LEFT BORDER	13	19
	342	342

VERTICAL	TMS 9918A/9928A LINE	TMS 9929A
VERTICAL ACTIVE DISPLAY	192	192
BOTTOM BORDER	24	50
BOTTOM BLANKING	3	3
VERTICAL SYNC	3	3
TOP BLANKING	13	13
TOP BORDER	27	52
	262	313

.7 VIDEO DISPLAY MODES

The VDP displays an image on the screen that can best be envisioned as a set of display planes sandwiched togethe Figure 2-6a shows the definition of each of the planes. Objects on planes closest to the viewer have higher priorit In cases where two entities on two different planes are occupying the same spot on the screen, the entity on t higher priority plane will show at that point. For an entity on a specific plane to show through, all planes in front that plane must be transparent at that point. The first 32 planes (Figure 2-6b) each may contain a single sprit (Sprites are pattern objects whose positions on the screen are defined by horizontal and vertical coordinates VRAM.) The areas of the Sprite Planes, outside of the sprite itself, are transparent. Since the coordinates of the spri are in terms of pixels, the sprite can be positioned and moved about very accurately. Sprites are available in thr sizes: 8 X 8 pixels, 16 X 16 pixels, and 32 X 32 pixels. Behind the Sprite Plane is the Pattern Plane. The Patte Plane is used for textual and graphics images generated by the Text, Graphics I, Graphics II, or Multicolor mode Behind the Pattern Plane is the backdrop, which is larger in area than the other planes so that it forms a bord around the other planes. The last and lowest priority plane of the TMS 9918A is the External VDP Plane. Its image is defined by t external VDP input pin. The backdrop consists of a single color used for the display borders and as the default col for the active display area. The default color is stored in the VDP register 7. When the backdrop color register co tains the transparent code, the backdrop automatically defaults to black if the external VDP mode is not selected. which does not exist in the TMS 9928A/9929A.

The 32 Sprite Planes are used for the 32 sprites in the Multicolor and Graphics modes. They are not used in the Te mode and are automatically transparent. Each of the sprites can cover an 8 X 3, 16 X 16, or 32 X 32 pixel area its plane. Any part of the plane not covered by the sprite is transparent. All or part of each sprite may also be tra parent. Sprite 0 is on the outside or highest plane, and sprite 31 is on the plane immediately adjacent to Patte Plane. Whenever a pixel in a Sprite Plane is transparent, the color of the next plane can be seen through that pla If, however, the sprite pixel is non-transparent, the colors of the lower planes are automatically replaced by the spr color. There is also a restriction on the number of sprites on a line. Only four sprites can be active on any horizon line. Additional sprites on a line will be automatically made transparent for that line. Only those sprites that a active on the display will cause the coincidence flag to set. The VDP status register provides a flag bit and t number of the fifth sprite whenever this occurs. The Pattern Plane is used in the Text, Multicolor, and Graph modes for display of the graphic patterns of characters. Whenever a pixel on the Pattern Plane is non-transparent, t backdrop color is automatically replaced by the Pattern Plane color. When a pixel in the Pattern Plane is transpare the backdrop color can be seen through the Pattern Plane.

TMS 9918A/9928A/9929A

This section describes the hardware and software interface between a ~~TMS 9918A~~ VDP and a TMS 9900 microprocessor. Also described are some of the considerations in the use of the ~~9918A~~ for text and graphics applications. Appendices in the back of this manual may also be referenced for software and hardware application examples for the VDP.

/9928A/9929A

VDP

TMS 9918A INTERFACE

VDP

Figure 3-1 shows the hardware components necessary to make the ~~9918A~~ operate. The CPU interface is shown disconnected because the VDP has a general-purpose, 8-bit data bus, and control signals that work with most microprocessors. The ~~TMS 9918A~~ interface timing is similar to that of static memories, and occupies eight unique memory address locations within the CPU memory address space.

VDP

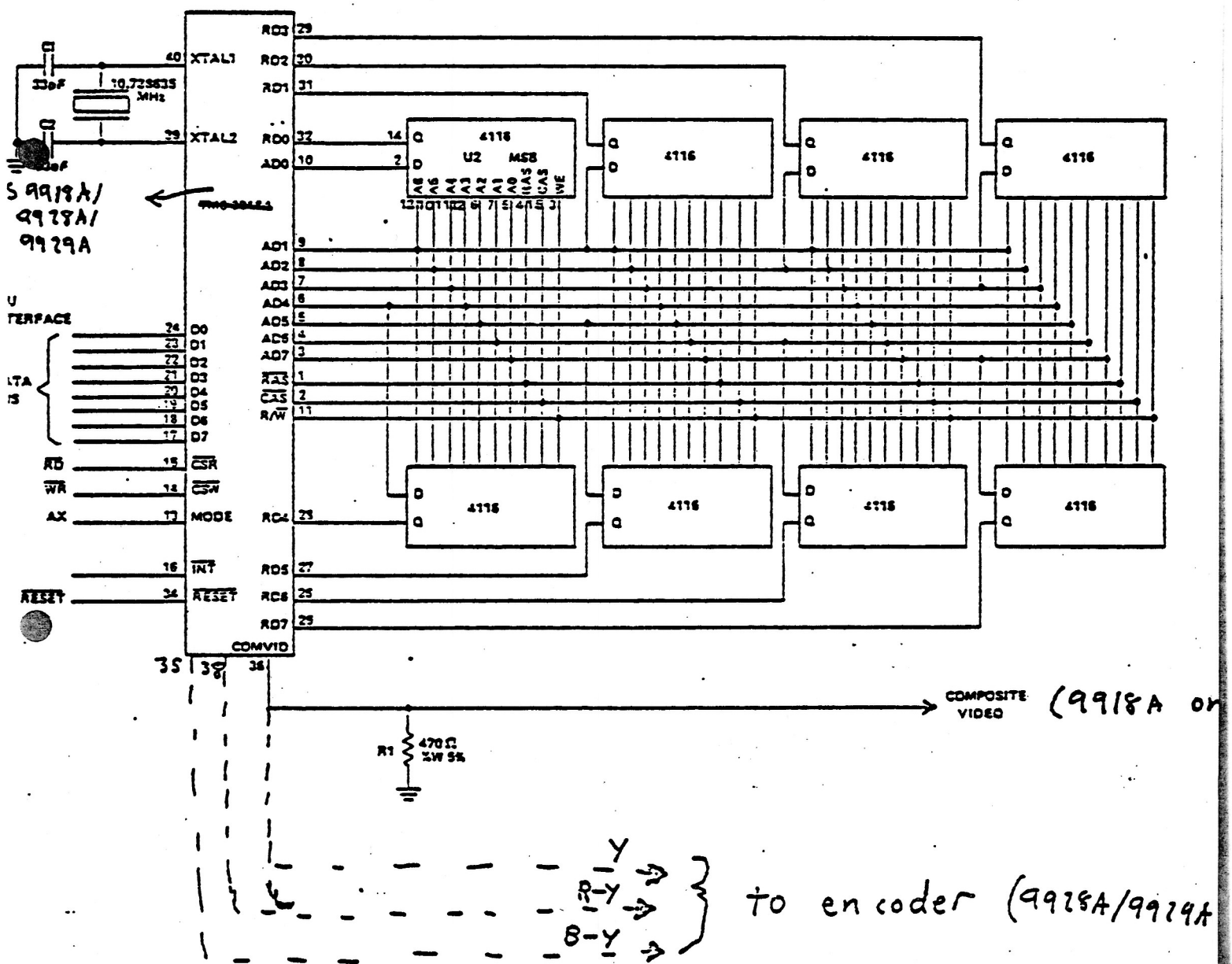
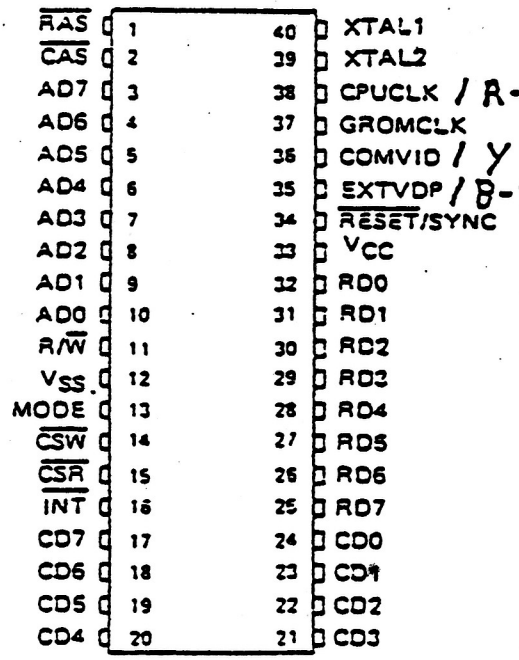


Figure 3-1 — TMS 9918A/9928A/9929A INTERFACE

VDP TERMINAL ASSIGNMENTS

SIGNATURE	TERMINAL	I/O	DESCRIPTION
D0 MSB	24	I/O	CPU data bus (CD0) is the most significant
D1	23	I/O	bit
D2	22	I/O	
D3	21	I/O	
D4	20	I/O	
D5	19	I/O	
D6	18	I/O	
D7	17	I/O	
ODE	13	I	CPU interface mode select; usually a processor address line
$\overline{SR}$	15	I	CPU-VDP read strobe
$\overline{SW}$	14	I	CPU-VDP write strobe
	33	I	+5 volt supply
S	12	I	Ground Reference
D0 MSB	32	I	VRAM read data bus (RD0 is the most signi-
D1	31	I	ficant bit)
D2	30	I	
D3	29	I	
D4	28	I	
D5	27	I	
D6	26	I	
D7	25	I	
D0 MSB	10	O	VRAM address/data bus (multiplexed high and low order VRAM address and output data bytes)
D1	9	O	AD0 is the most significant bit and is used only for data and not for addressing.*
D2	8	O	
D3	7	O	
D4	6	O	
D5	5	O	
D6	4	O	
D7	3	O	
$\overline{AS}$	1	O	VRAM row address strobe
$\overline{AS}$	2	O	VRAM column address strobe
$\overline{W}$	11	O	VRAM write strobe
TAL1, TAL2	40,39	I	10.7 ÷ MHz crystal inputs.**
ROMCLK	37	O	VDP output clock = XTAL/24. Typically not used
$\overline{RESET}$/SYNC	34	I	$\overline{RESET}$—This pin is a trilevel input pin. When it is below 0.8 volts, $\overline{RESET}$ initializes the VDP. When it is above 9 volts, $\overline{RESET}$ is the synchronizing input for external video.



RE	TERMINAL	I/O	DESCRIPTION
UP/B-Y	35	I/O	External VDP input
PUCLK/R-Y	38	O	Color burst frequency clock. Typically not used.
IT	16	O	CPU interrupt output.
OMVID/Y	36	O	Composite video output.

The least-significant address bit, AD7, is wired to A0 of the dynamic RAMs. Likewise, AD6 is wired to A1 of the RAMs. Care must be exercised in assuring proper orientation of the 9918A address outputs to the dynamic RAM address inputs. When driven externally, both inputs must be driven.

Note: Crystals for the TMS 9918A/9928A/9929A may be purchased from one of the following companies or authorized distributors:

NDK
10080 North Wolfe Rd
Suite 220
Cupertino, CA 95014
Tele: (408) 255-0931
Telex: 352057

CTS Knights, Inc
400 Reimann Ave
Sandwich, ILL 60548
Tele: (815) 786-8411

On the TMS 9918A this is the external VDP input on the TMS 9928A/9929A this is the B-y color difference o

on the TMS 9918A this is the color burst frequency clock and is typically not used.
on the TMS 9928A/9929A this is the R-y color difference output

Composite video output for the TMS 9918A. On the TMS 9928A/9929A this is the Y (black/white luminance and composite sync) output.

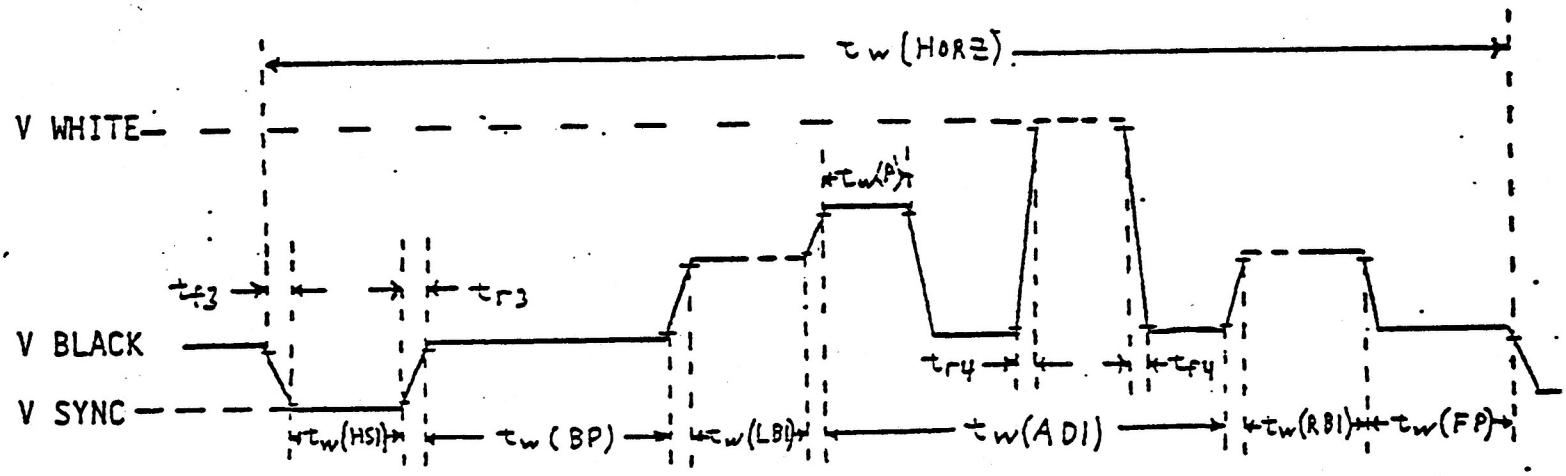


FIGURE 4-9 - TMS 9928A/9929A Y HORIZONTAL TIMING

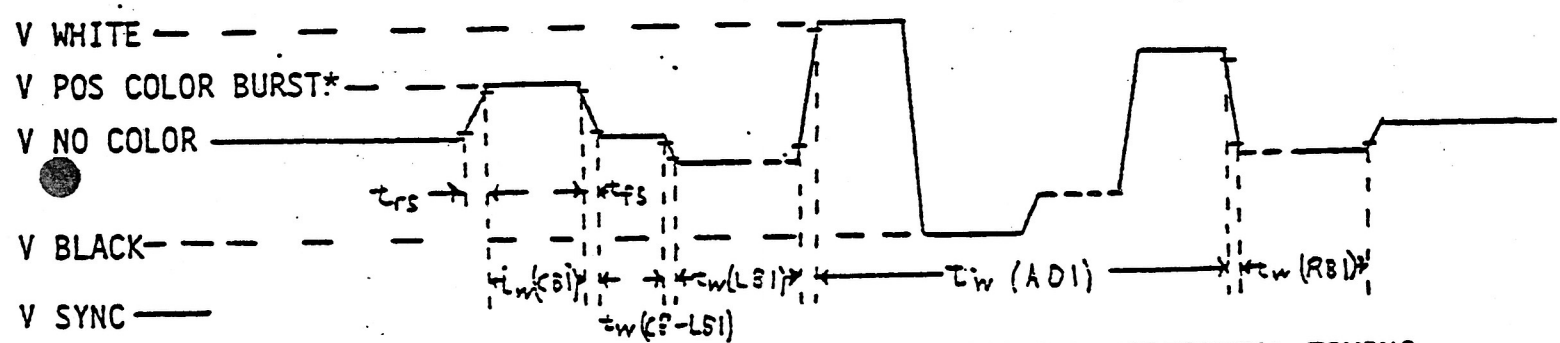


FIGURE 4-10 - TMS 9928A/9929A R-Y HORIZONTAL TIMING
* Absent for the 9928A

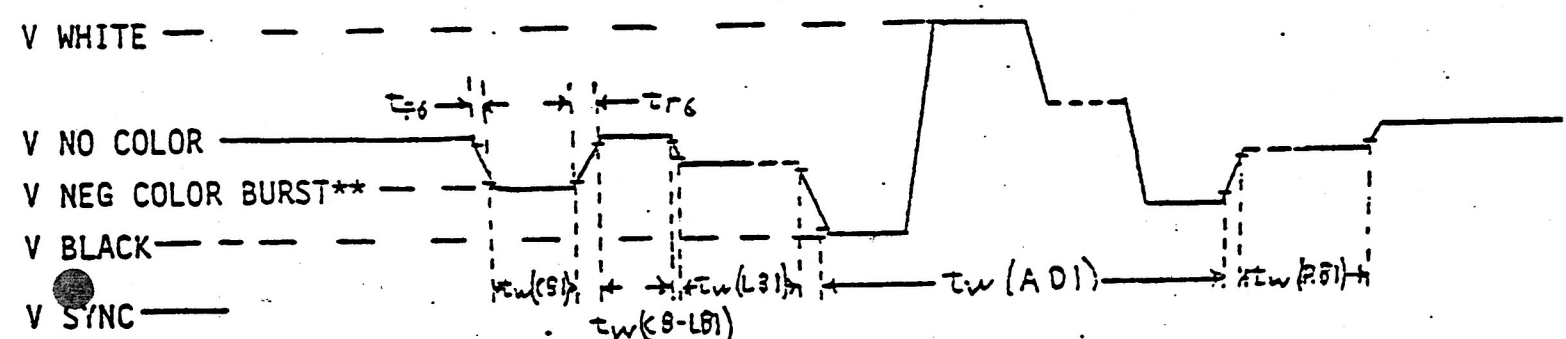
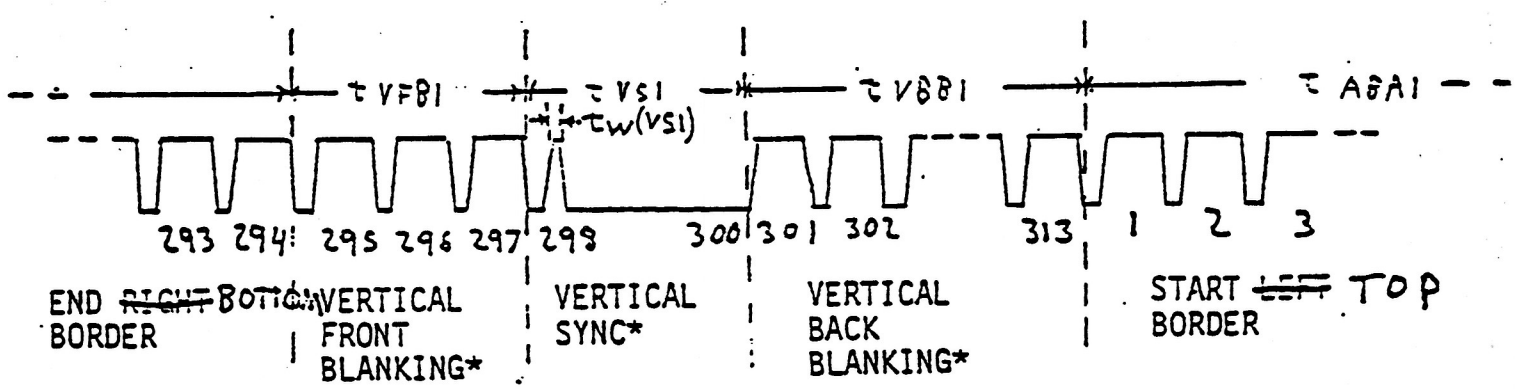


FIGURE 4-11 - TMS 9928A/9929A B-Y HORIZONTAL TIMING
** Amplitude changes for the 9928A (see spec)



* COLOR BURST OUTPUT SUPPRESSED
FIGURE 4-12 - TMS 9929A VERTICAL TIMING

TMS 9918A/9928A/9929A PRELIMINARY ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (unless otherwise noted)*

Supply voltage, V_{CC}	−0.3 to 20 V
All input voltages	−0.3 to 20 V
Output voltage	−2 to 7 V
Continuous power dissipation	1.8 W
Operating free-air temperature range	0°C to 55°C
Storage temperature range	−55°C to +150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS*

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Supply voltage, V_{SS}			0		V
Input voltage, V_I, $\overline{RESET}$/SYNC pin	SYNC active	10		12	V
	RESET active	0		0.6	
	SYNC and RESET inactive	3		6	
High-level input voltage, V_{IH}	XTAL1, XTAL2	2.75			V
	All other inputs	2.2			V
Input voltage, V_I, EXTVDP pin (9928A only)	SYNC level		2.5		V
	White level		3.7		
	Black level		3		
Low-level input voltage, V_{IL}		0		0.8	V
Operating free-air temperature, T_A		0		55	°C

*Voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS OVER FULL RANGES OF RECOMMENDED OPERATING CONDITIONS (unless otherwise noted)

	PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	RAS, CAS, R/W	I_{OH} = −400 µA		2.7			V
		All other outputs			2.4			
V_{OL}	Low-level output voltage	CPU data	I_{OL} = 1.2 mA				0.6	V
		DRAM interface	I_{OL} = 800 µA				0.6	
I_{OZH}	Off-state output current high-level voltage applied, D0-D7 outputs		V_O = 5.5 V				100	µA
I_{OZL}	Off-state output current low-level voltage applied, D0-D7 outputs		V_O = 0 V				−100	µA
I_I	High-level input current		V_I = 5.5 V,	All other pins at 0 V			10	µA
	Low-level input current		V_I = 0 V,	All other pins at 0 V			−10	µA
WHITE	Video voltage level of white, COMVID output Y/R-Y/B-Y outputs				2.5	3		V
BLACK	Video voltage level of black (blank), COMVID output Y/R-Y - B-Y outputs					2.3		V
SYNC	Video voltage level of sync, COMVID output Y outputs					1.9		V
$V_{CB(P-P)}$	Video voltage (peak-to-peak) of burst, COMVID output 9918A					0.5		V
	Video voltage difference, white − black, COMVID output Y/R-Y/B-Y outputs				0.5	0.7		V
I_{CC}	Average supply current from V_{CC}		T_A = 25°C			200	250	mA
C_i	Input capacitance	D0-D7	f = 1 MHz,	Unmeasured pins at 0 V			20	pF
		All other inputs					10	
C_o	Output capacitance		f = 1 MHz,	Unmeasured pins at 0 V			20	pF

†Typical values are at V_{CC} = 5.25 V, T_A = 25°C.

			TYP	
V_{POS} color burst	Video voltage level	of B-Y output	.25	V
V_{NEG} color burst	Video voltage level	of B-Y output	−.25	V

TMS 9928A/9929A Y, R-Y, B-Y OUTPUTS

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
tf3	Fall time, V BLACK to V SYNC				100	n sec.
tw (HS1)	Pulse width, Horizontal SYNC			4.84		u sec.
tr3	Rise time, V SYNC to V BLACK				150	n sec.
tw (BP)	Width, Back Porch			4.47		u sec.
tw (LB1)	Width, Left Border			2.8		u sec.
tw (P)	Pulse width, Pixel			186.24		n sec.
tw (HORZ)	Width, Horizontal Line			63.695		u sec.
tw (AD1)	Width, Active Display Area			47.67		u sec.
tr4	Rise time, V BLACK to V WHITE				75	n sec.
tf4	Fall time, V WHITE to V BLACK	$R_L = 560\Omega$			50	n sec.
tw (RB1)	Width, Right Border	$C_L = 150$ pF		2.42		u sec.
tw (FP)	Width, Front Porch	see figure 4-8		1.49		u sec.
tr5	Rise time, V NO COLOR to V POS CB		0		150	n sec.
tw (CB1)	Pulse width, POS COLOR BURST				2.6	u sec.
tf	Fall time, V POS CB to V NO COLOR		0		100	n sec.
tw (CB-LB1)	Delay time, POS CB to LEFT BORDER			1.49		u sec.
tf6	Fall time, V NO COLOR to V NEG CB				100	n sec.
tr6	Rise time, V NEG CB to V NO COLOR				150	n sec.
tw (VS1)	Pulse width, Vertical SYNC				465	n sec.
VFB1	VERTICAL FRONT BLANKING			191.09		u sec.
VS1	VERTICAL SYNC			191.09		u sec.
VBB1	VERTICAL BACK BLANKING			828.04		u sec.
ABA1	ACTIVE AREA PLUS BORDER AREA			18.70		m sec.
	TOTAL VERTICAL TIME			19.91		m sec.

ote fall times depend on external pull-down resistor.